6502A CPU BOARD

UNIT DESCRIPTION

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TABLES

FIGURES

1. INTRODUCTION

1.1 GENERAL

The 6502A CPU Board provides the Central Processor Unit (CPU) for a modular computer system. The CPU is constructed on a 100 x 160mm Eurocard which plugs into a standard Eurocard rack. A 6502A Microprocessor (µP) is run at 1, 2 or 3MHz from a 24MHz crystal controlled clock to provide the following CPU functions, refer also to the block diagram, Figure 1:

— *Read Only Memory (ROM).* A 28-pin DIL socket is provided for the installation of a ROM IC for the resident software. Links are wired on a header inserted in a 16-pin DIL socket to cater for a large range of 28-pin or 24-pin ROM ICs.

— *Random Access Memory (RAM).* A 24-pin DIL socket is provided for a 6116 2K x 8 bit static RAM IC. The RAM provides the stack and user memory areas. Other optional ICs such as 4118 may be used.

— *Input/Output (I/O).* A 6522A Versatile Interface Adaptor (VIA) IC fitted to the CPU Board provides two I/O Ports. The VIA Port (A) is connected to PL1 to provide an interface with an external unit such as a Keyboard. The VIA Port (B) is connected to PL2 to provide a User Port.

The CPU address, data and control lines are buffered for connection to the standard Acorn Bus via PL2. Additional interrupt and Direct Memory Access (DMA) lines are also connected to PL2, as are the System Clock outputs.

1.2 LEADING PARTICULARS

1.2.1 Mechanical

Construction : Single Eurocard printed circuit board.

Size : 100mm x 160mm

1.2.2 Power Supplies

+5V ± 5% at 520mA typically.

1.2.3 Connections
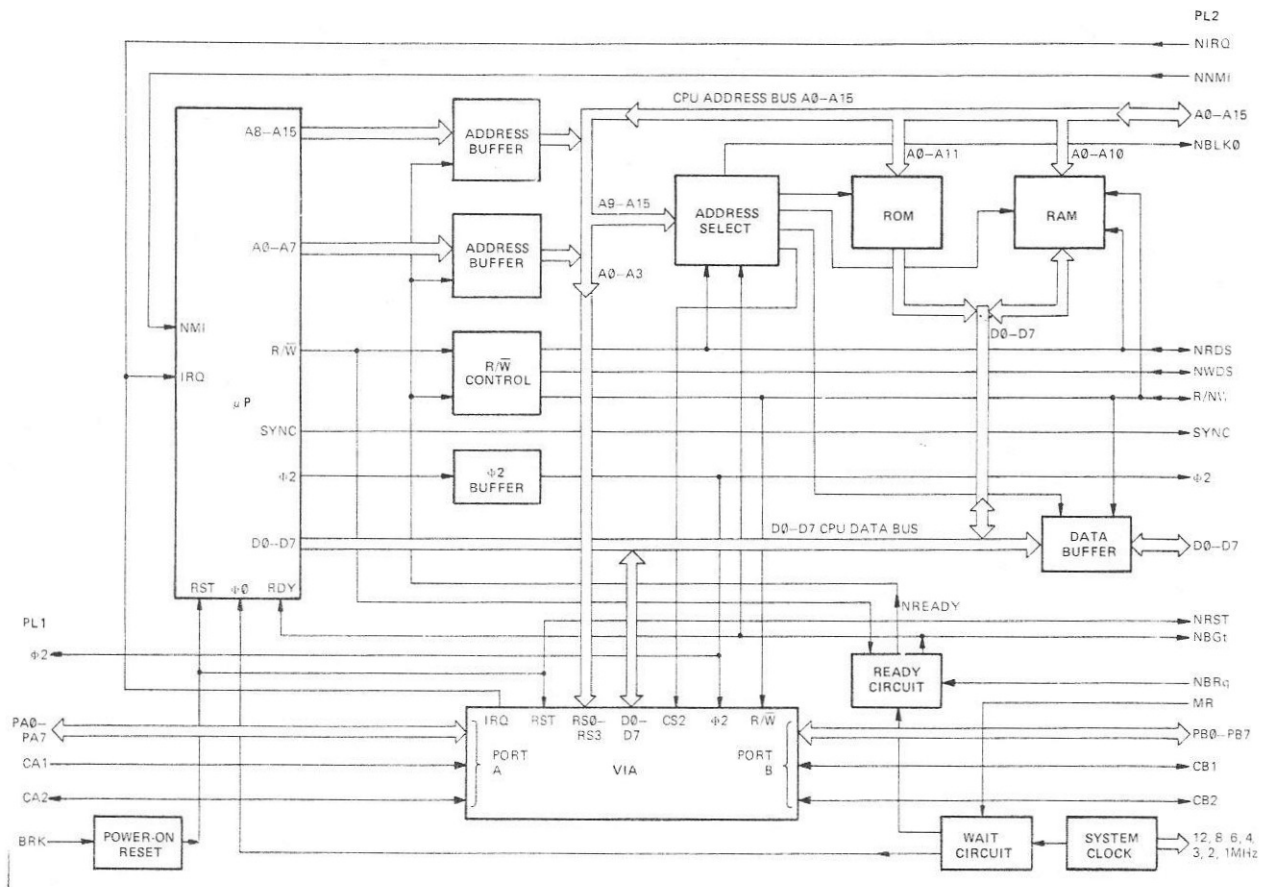
Pin connections are given in Section 4.
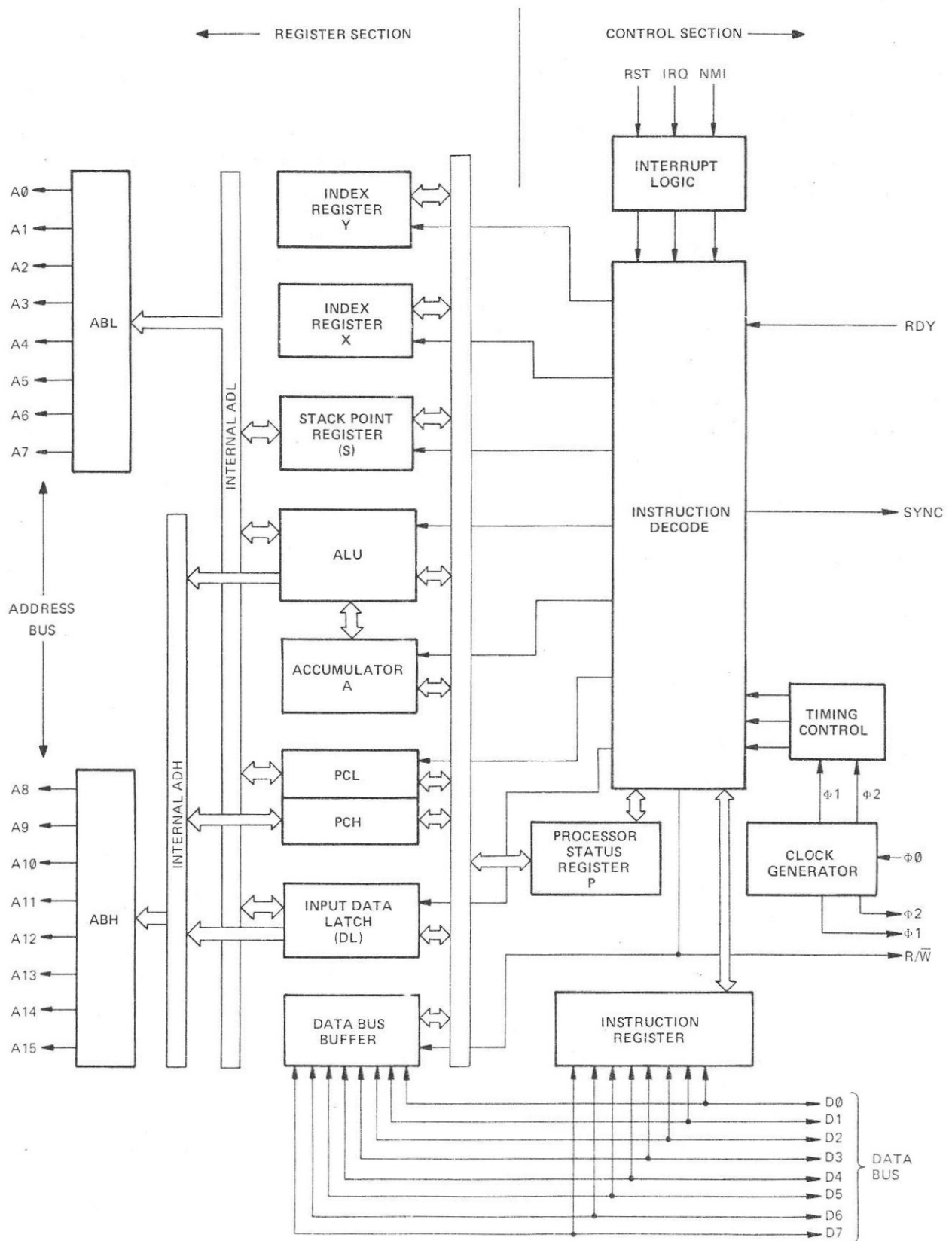

Figure 1. 6502A CPU Board Block Diagram

Figure 2. 6502A Microprocessor Internal Architecture

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Connectors : Double sided edge connector to Acorn Bus, TTL signal levels are used, DV to 0.4V = logic 0, >=+2.4V logic 1.

20-way connector for external unit, i.e. Keyboard. TTL signal levels are used, 0V to 0.4V = logic 0, => +2.4V = logic 1.

2. CIRCUIT DESCRIPTION

The circuit diagram for the CPU Board is given on Figure 21 (filed at the end of this section) and should be referred to in conjunction with the description.

2.1 MICROPROCESSOR

The 6502A Microprocessor (µP) IC8 operates at 1MHz, 2MHz or 3MHz, depending upon the setting of links LK1, LK2 and LK3. The microprocessor has a 16 bit address bus and an 8 bit bi-directional data bus. CPU control is provided by the Read/Write (R/W) and clock (§2) output signals, refer to block diagram, Figure 2. Two interrupt inputs are provided, Interrupt Request (NIRQ) and Non-Maskable Interrupt (NNMI). Power-on reset, ready and synchronization connections are also provided.
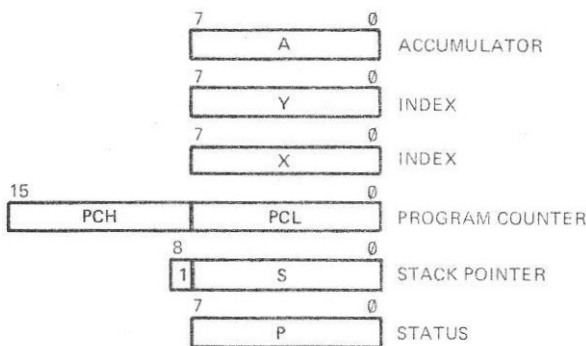
(a) Programming Model
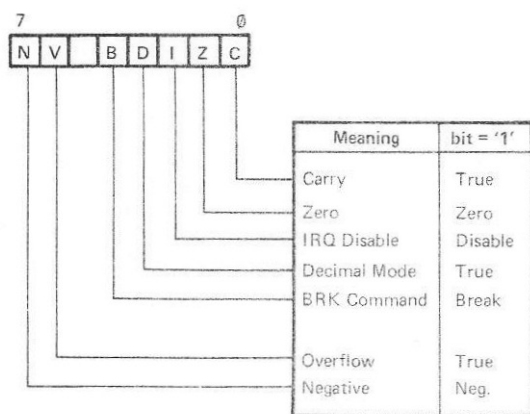
(b) P Register Bit Significance

Figure 3. Microprocessor Registers

The microprocessor address lines are buffered by IC9 and IC10. IC15 buffers the §2 and R/W lines.

2.1.1 Microprocessor Registers

The 6502A Microprocessor internal registers are as shown on Figure 3. The functions of the registers are as follows:

- *Accumulator (A).* An 8 bit general purpose register used with the Arithmetic Logic Unit (ALU) for instruction execution. The A Register contents are not saved when an interrupt occurs.

- *Index (X and* Y). Two 8 bit index registers are provided. These registers are used for indexed addressing, a 16 bit offset can be used. The X and Y Register contents are not saved when an interrupt occurs.

- *Program Counter (PC).* A 16 hit register for the address of the instruction to be executed.

- *Stack Pointer (S).* A 9 bit register for the current stack address. On reset the S Register contains the address 01FF Hexadecimal (hex).

- Status (P), An 8 bit register that contains the microprocessor flags, refer to Figure 3. A '1' is loaded into the appropriate flag bit when a condition is true.

2.1.2 Microprocessor Inputs and Outputs

The functions of the microprocessor inputs and outputs are as follows:

ADDRESS LINES : A0—A15
These 16 lines are used to carry the address output from the microprocessor. The address lines are buffered onto the CPU Address Bus and the Acorn Bus by IC9 and IC10. The NREADY signal low from the Ready bistable IC5/6, enables IC9 and IC10, refer to para 2.5. When the NREADY signal is high, the outputs of IC9 and IC10 are disabled (high impedance) to allow external DMA control of the CPU Board Address Bus via the Acorn Bus.

DATA LINES : D0—D7
These 8 lines are used to carry the 8 bit data bytes to or from the CPU Data Bus. The CPU Data Bus is connected directly to the ROM IC11, the RAM IC13, the VIA IC7, and through the Data Buffer IC12, to the Acorn Bus.

READ/WRITE : R/W
The R/W signal is used to identify the direction of data transfer on the data lines. The R/W signal is high for data transfer to the microprocessor and low for data output from the microprocessor. The timing of the R/W signal is given on Figure 4. The R/W signal is buffered to the Acorn Bus by IC15/3, refer to Read/ Write Control, para 2.6.

CLOCK INPUT : §0
The §0 clock input drives the microprocessor clock circuits at the frequency selected, refer to para 2.3.

CLOCK OUTPUT : §2
The §2 clock output is derived internally by the microprocessor from the §0 input. §2 is in phase with §0, refer to the timing diagram, Figure 4 (§1 is not used on the CPU Board). The §2 signal is buffered by IC15/11 to the CPU Board and the Acorn Bus.

SYNC
The SYNC signal is used to identify the microprocessor, instruction fetch cycles. The timing of the SYNC signal is shown on Figure 4. The SYNC signal may be used in conjunction with the RDY signal to induce a microprocessor halt state, see RDY below.
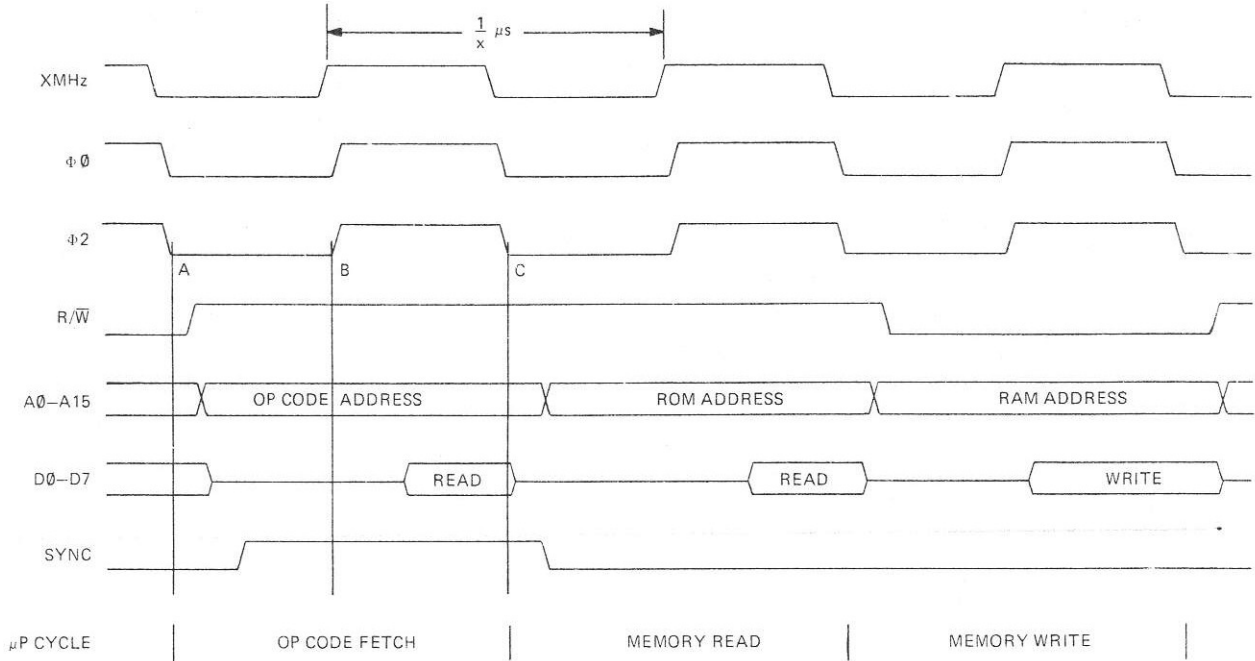
Figure 4.   Microprocessor Signal Timing
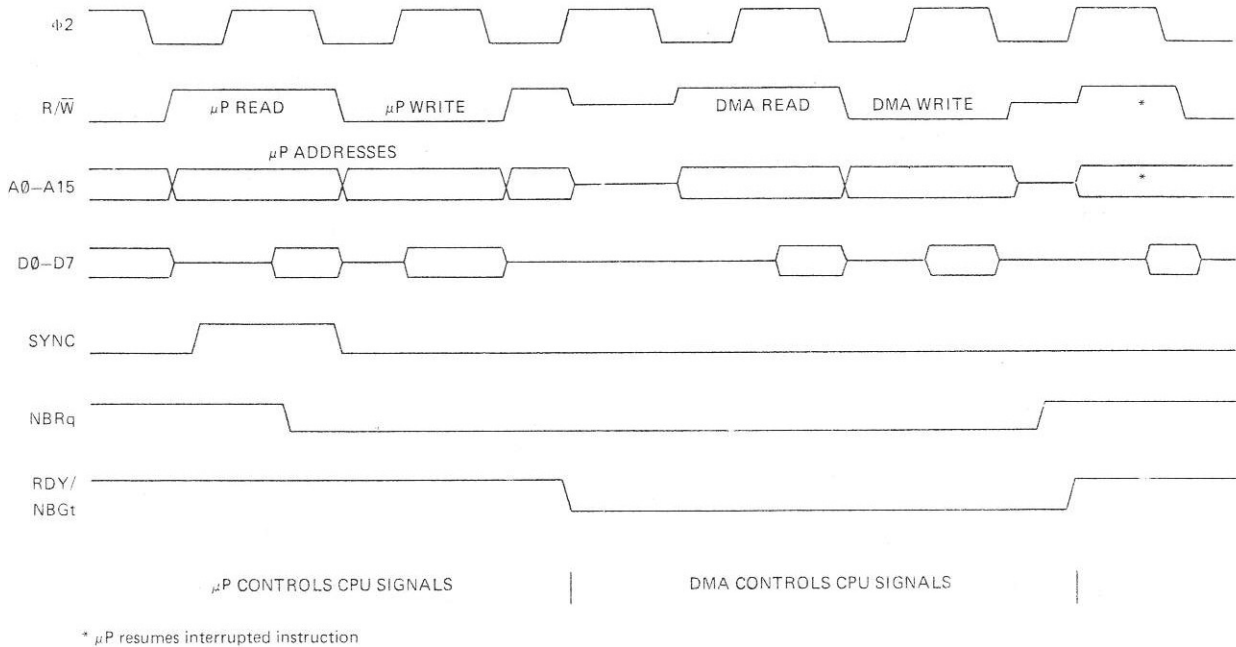
Figure 5. DMA Timing (CPU Board Signals)

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READY SIGNAL : RDY

The RDY input signal to the microprocessor is normally high. When the microprocessor is used for DMA operations, a low input on the RDY line halts the microprocessor with the current address on the address lines, refer to para 2.5. If the microprocessor is executing a write cycle, the RDY signal is not set until the end of the cycle. Figure 5 shows a typical DMA operation with a halt state.

INTERRUPTS : NIRQ, NNMI

The microprocessor has two interrupt inputs, Interrupt Request (NIRQ) and Non-Maskable Interrupt (NNMI).

The NIRQ signal low is sampled at §2 time and if not masked by the interrupt mask flag, begin the interrupt sequence at the next microprocessor machine cycle, refer to para 3.3.1. The vectored addresses are loaded from memory locations FFFE and FFFF (hex).

The NNMI signal going low initiates an unconditional interrupt, which is otherwise similar to the NIRQ interrupt, refer to para 3.3.2. The vectored addresses in this case are loaded from memory locations FFFA and FFFB (hex).

RESET : RST

The RST input is used to reset the microprocessor, or start the microprocessor from a power down condition. The NRST signal is held low on power-up for approximately 10ms, a positive edge then initiates a reset sequence, refer to para 3.3.3. An external reset can be initiated by applying 0V to PL1 pin 15, refer to para 2,11.

2.2   ADDRESS SELECT

The Address Select circuits provide address line decoding in normal microprocessor and DMA operation, for the RAM and ROM fitted to the CPU Board, and also for the VIA. Links are used to change the signals applied to the ROM pins to cater for different ROM ICs, IC13 position may be used for an additional ROM IC, which is then selected by the RAM Select circuit.

2.2.1 RAM and VIA Selection

The RAM and VIA Select circuit is shown on Figure 6. IC20 is a dual two line decoder. IC20a is enabled by the Block 0 address, address lines A12—A15 all ' 0's (0 hex). The output from IC6/C is also connected to PL2 pin 31b to generate the NBLK0 signal low on the Acorn Bus.
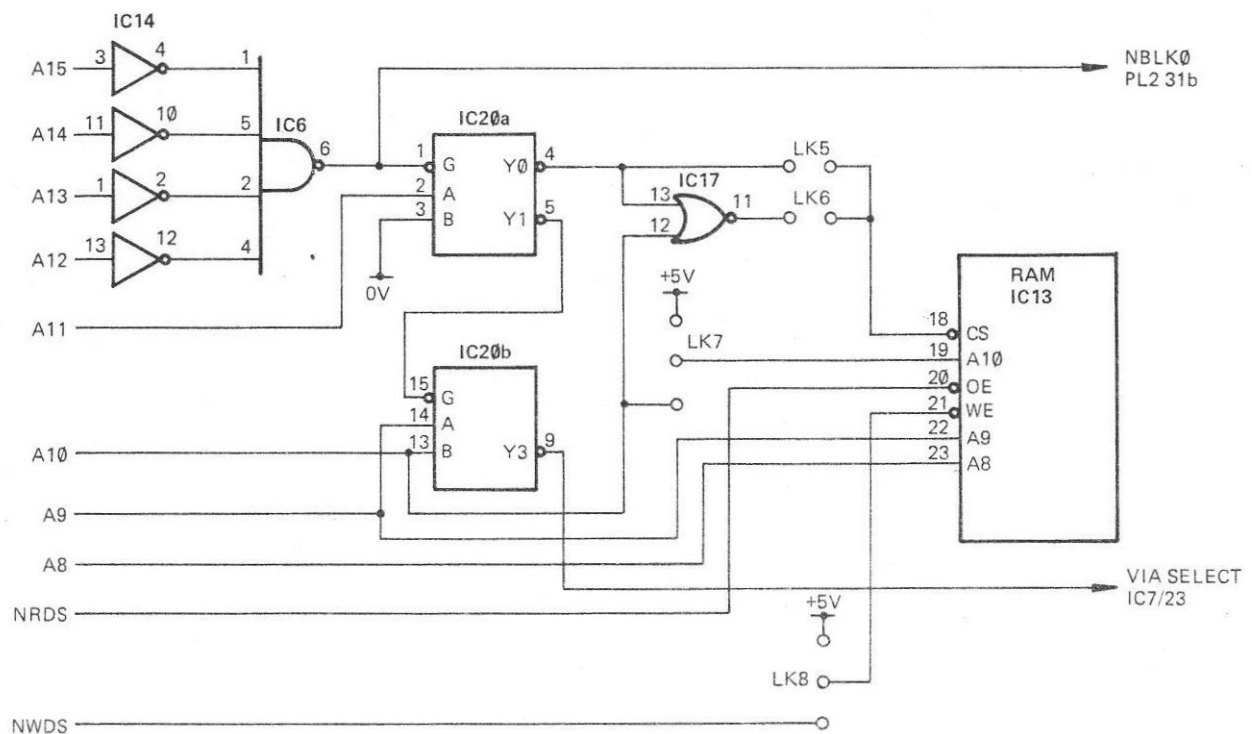
Figure 6. RAM and VIA Select Circuit
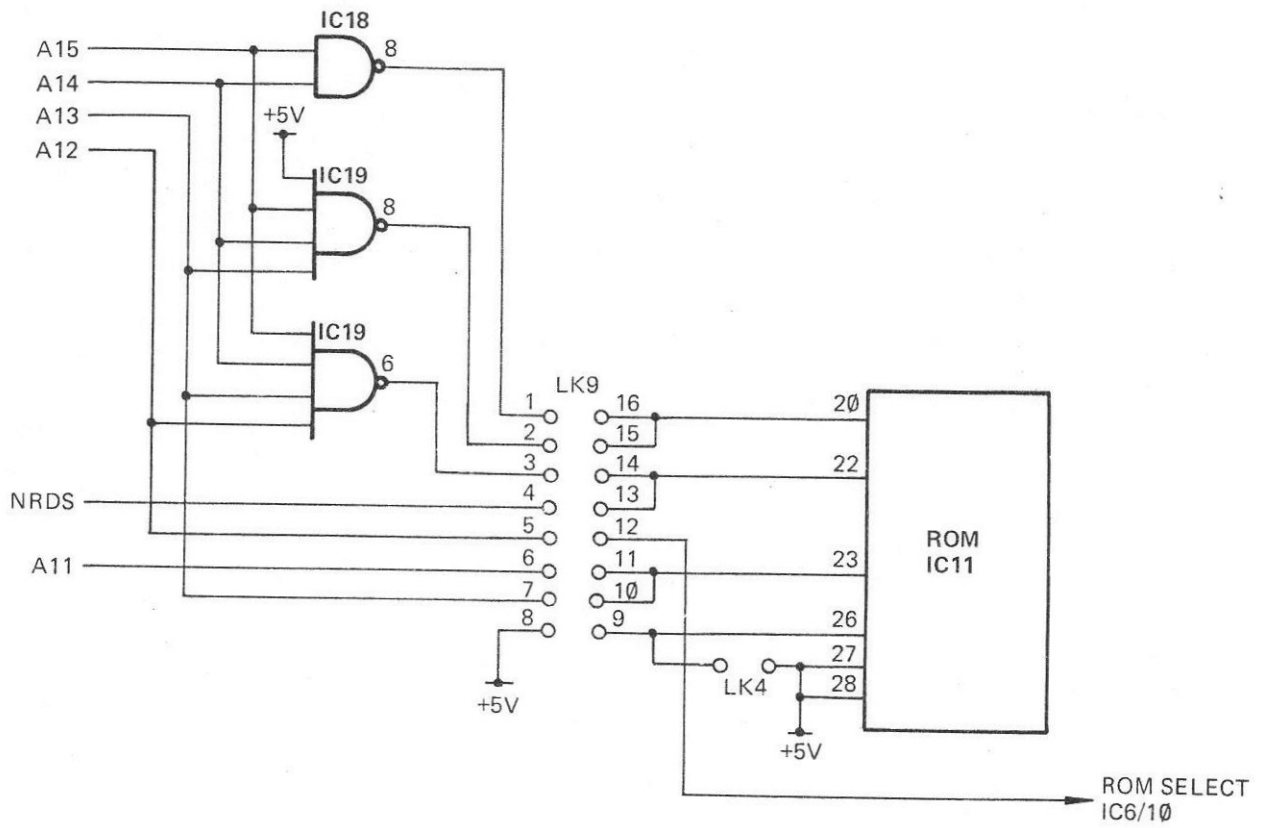
Figure 7. ROM Select Circuit

(a) Synertek 2332

(b) Texas 2532

(c) Intel 2732 or Intel 2732A

(d) Synertek 2364

(e) Intel 2764

(f) Synertek 23128

(g) Synertek 2316

(h) Texas 2516

(i) Mostek 2716
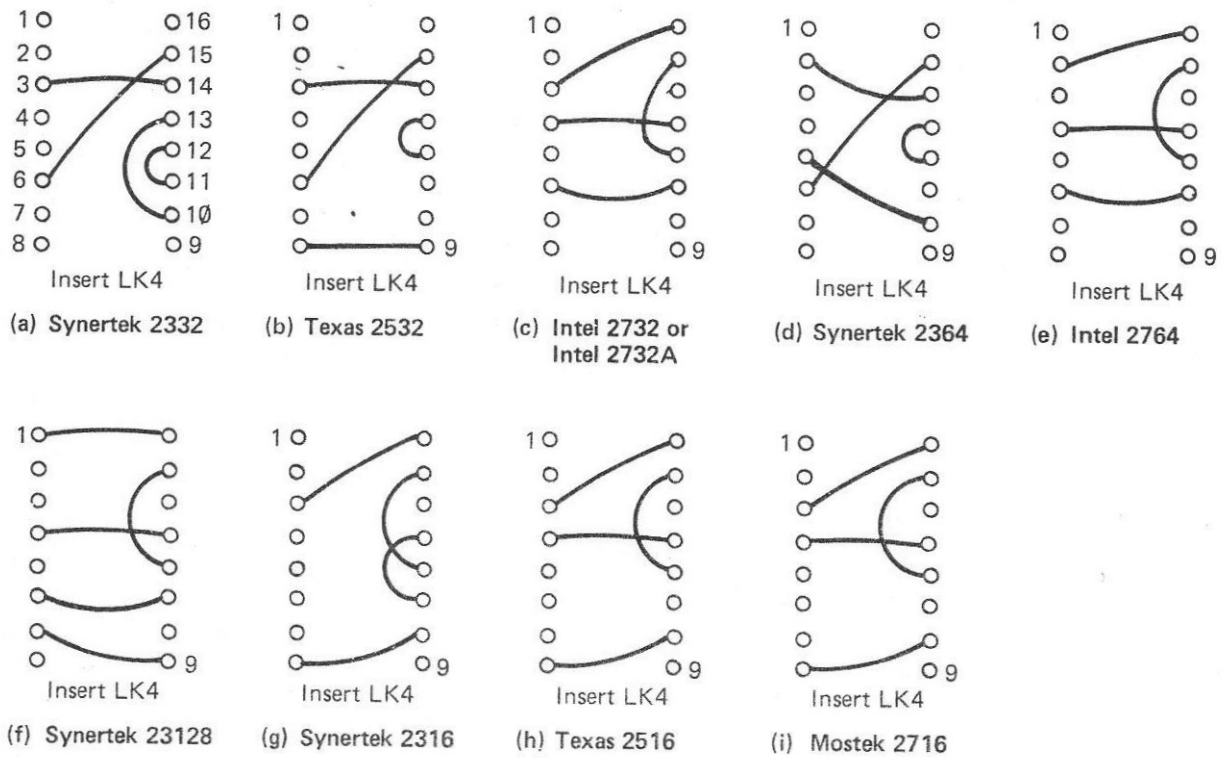
Figure 8. LK9 and LK4 Configurations

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Address line A11 low generates a low on the Y0 output IC20/4, to select the RAM IC13, either via LK5, or via OR gate IC17/11 and LK6. LK5 is inserted when 2K of RAM is required in Block 0, addresses 0000 to 07FF (hex). When only 1K of RAM is required, LK6 is inserted and the RAM is selected for addresses 0000 to 03FF (hex) by address line A10 low at the OR gate. A10 high inhibits the RAM selection for addresses 0400 to 07FF (hex). The RAM select signal from LK5 or LK6 also inhibits the I/O Data Buffer for microprocessor RAM operations, refer to para 2.9.

The Y1 output of IC20a enables IC20b. IC20b decodes A10 and A9, both lines '1', to produce a low on the Y3 output IC20/9 and select the VIA for addresses 0E00 to 0FFF (hex). IC20/9 low also inhibits the I/O Data Buffer when the VIA is selected for microprocessor operations, refer to para 2.9.

Two links LK7 and LK8 are provided on the CPU Board to permit the use of other RAM or ROM ICs in the IC13 socket. The track on the Board has to be cut and links soldered to use this facility. LK8 connects pin 21 to +5V instead of NWDS and LK9 connects pin 19 to +5V instead of A10.

When a 4118 RAM IC is used in IC13, LK7 is connected to +5V and LK6 link inserted to give addresses 0000 to 03FF (hex) for the RAM.

The IC13 position can be used for ROM ICs. In this case LK8 is connected to +5V and LK5 link inserted to give addresses 0000 to 07FF (hex) for the ROM. Suitable ICs are 2516 and 2716.

2.2.2   ROM Selection

The ROM Select circuit is shown on Figure 7. The LK9 links are wired on a 16-pin DIL header that is inserted in the DIL socket. The link patterns for the various types of ROM IC which may be fitted in the IC11 socket, are shown on Figure 8. A link is also inserted in or removed from LK4 as indicated on Figure 8. The connection to LK9 pin 12 is used to inhibit the I/O Data Buffer during microprocessor memory read operations, refer to para 2.9.

The output of IC18/8 is low at LK9 pin 1 for all addresses in the range C000 to FFFF (hex) on the address lines.

The output of IC19/8 is low at LK9 pin 2 for all addresses in the range E000 to FFFF (hex) on the address lines.

The output of IC19/6 is low at LK9 pin 3 for all addresses in the range F000 to FFFF (hex) on the address lines.

The address lines A11 to A13 are connected to the appropriate pins on the ROM via links from LK9 pin 6, 5 and 7 respectively.

Signal NRDS is connected to the appropriate output enable (OE) pin on the ROM via a link from LK9 pin 4.

2.3   SYSTEM CLOCK

The System Clock is driven by the 24MHz crystal oscillator circuit X1, IC1, C3, R9, R10 and R13. Synchronous binary counters IC2, IC3 and IC4 divide the 24MHz clock signal output of the oscillator to produce: 12, 8, 6, 4, 3, 2 and 1MHz clock signals. The clock signals are synchronized to the falling edge of the 1MHz signal, refer to Figure 9. The microprocessor clock frequency is selected by a link as follows:

Link	Frequency
LK2	1MHz
LK3	2MHz
LK1	3MHz

The counter IC2 is configured to divide the 24MHz clock signal by three. The QB output is inverted by IC1 to clear IC2 every third clock pulse, refer to timing diagram, Figure 9. The IC2 QA output (8MHz) is connected to the enable P and T inputs of IC3, as well as to PL2 pin 14b via R15 (8MHz Acorn Bus clock).

The IC2 QA output is connected to the enable P and T inputs of counter IC3, so that IC3 counts every third 24MHz clock pulse. The QA, QB and QC outputs produce the 4, 2 and 1MHz clock signals. The 2 and 1MHz signals are connected to links LK2 and LK3 respectively, to provide the required microprocessor §0 clock input via the Wait Circuit, refer to para 2.4. The 4, 2 and 1MHz clock signals are output via R17, R19 and R20 onto the Acorn Bus via PL2 pins 16b, 18b and 19b respectively. The IC3 carry output is used to synchronize IC4.

The counter IC4 divides the 24MHz clock signal to produce 12, 6 and 3MHz outputs at QA, QB and QC. The 3MHz output is connected to link LK1 to provide the microprocessor §0 clock input if required. The 12, 6 and 3MHz clock signals are output via R14, R16 and R18 onto the Acorn Bus via PL2

pins 13b, 15b and 17b respectively. The carry output of IC3 is inverted by IC1 to clear IC4 every 2µs, thus ensuring that the IC4 outputs are synchronized to the 1MHz clock output from IC3, refer to timing diagram, Figure 9. Note that the IC3 carry output remains low, until the 8MHz clock signal at the enable T input goes high.

2.4   WAIT CIRCUIT

The Wait Circuit provides the means for stopping the microprocessor for slow memory or peripheral operations. While the Memory Ready (MR) signal is high at PL2 pin 26b, the high on IC5/12 gives a low on the Q output pin IC5/8, so that the selected clock from link LK1, 2 or 3 is output from OR gate IC17/8. When signal MR goes low, the next positive going clock signal clears the Q output IC5/8 high to IC17/9. This applies a high on the microprocessor §0 input to stop the microprocessor. When MR goes high again IC5/8 is set low and the clock output to the microprocessor is enabled.

2.5   READY CIRCUIT

The Ready Circuit is used to introduce a halt state in the microprocessor for DMA operations.

While the Bus Request signal NBRq on the Acorn Bus is high at PL2 pin 25b, or the pin is open circuit (R7 pulls-up IC1/9), IC18/5 low applies a high to IC5/2. The Q output IC5/5 sets the microprocessor RDY input high to allow normal operations. This signal is also output on the Acorn Bus as the Bus Grant signal NBGt at PL2 pin 22b. -

When NBRq goes low and the microprocessor R/W signal output is high (read), IC18/6 goes low, so that the next positive edge of the §0 clock from IC17/8 will reset IC5 Q output low. The low on the microprocessor RDY input induces a halt state, refer to Figure 5.

The Q output from IC5/6 inhibits the R/NW, NRDS and NWDS signals from buffers IC15 and the address line buffers IC9 and IC10, during the halt state, the buffer outputs go high impedance. When NBRq goes high the next positive edge of §0 sets the Q output IC5/5 high, to generate the RDY signal high and end the microprocessor halt state.

2.6   READ/WRITE CONTROL

The Read/Write Control Circuit buffers the microprocessor R/NW output from IC8/34 and generates the NRDS and NWDS signals for the Acorn Bus. The circuit is shown on Figure 10.
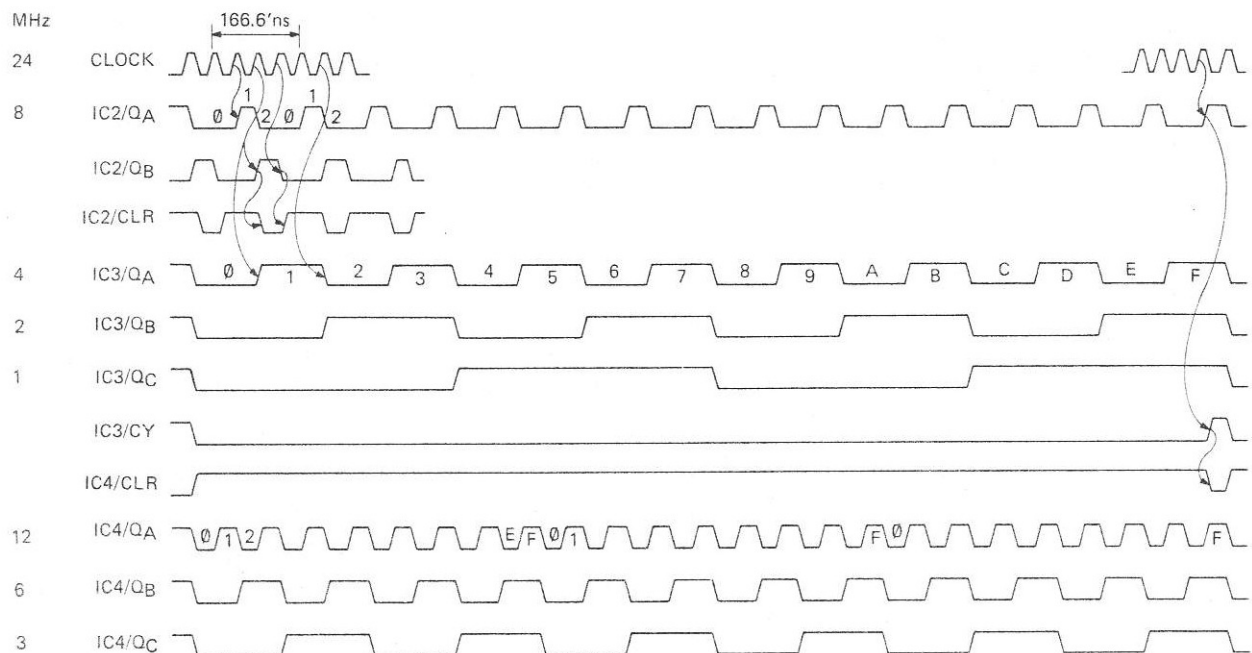
Figure 9. System Clock Timing Diagram
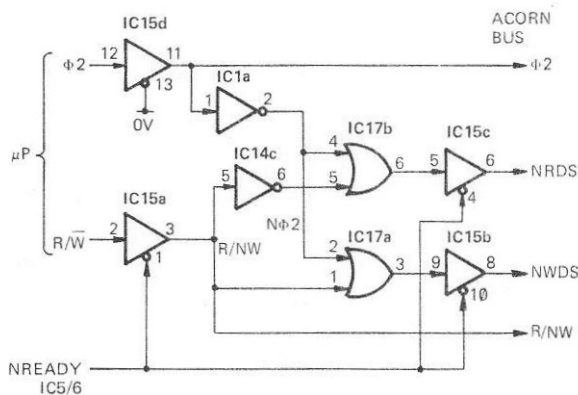
Figure 10. Read/Write Control Circuit

The §2 clock output from the microprocessor is buffered by IC15d and inverted by IC1a to enable IC17a and IC17b at each §2 clock time. The R/W signal output from the microprocessor is buffered by IC15a, then connected directly to IC17a and via inverter IC14c to IC17b. The Read and Write Control signals thus produced are buffered by IC15c and IC15b to generate the Read Strobe (NRDS) and Write Strobe (NWDS) signals for the Acorn Bus, refer to timing diagram, Figure 11. The IC5/6 Q output (N READY) high disables the buffers to the high impedance output state, to allow DMA control of the WNW, NR DS and NWDS Acorn Bus lines.

* high impedance output
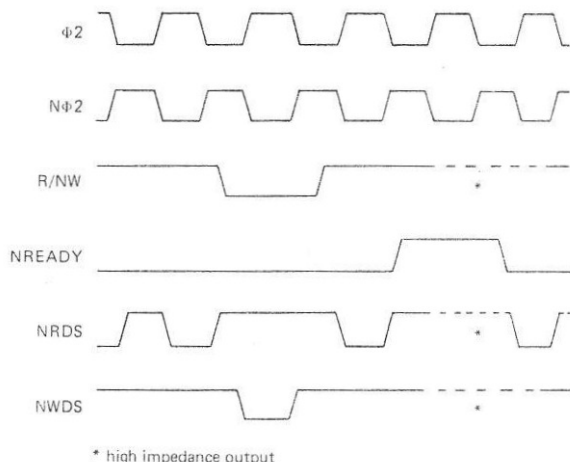
Figure 11. NRDS and NWDS Timing

2.7   READ ONLY MEMORY

The Read Only Memory (ROM) is selected by address lines A12—A15, refer to para 2.2.2. Various ROM ICs may be equipped in the IC11 position. IC13 may also be equipped with a ROM. When selected, address lines A0—A13 select the required location in the ROM, refer to para 2.2.2 and Figures 7 and 8 for

details of particular ROM address line connections. The data from the addressed location is output onto data lines D0—D7 by the NRDS signal low. When not selected the ROM data outputs are high impedance.

2.8   RANDOM ACCESS MEMORY

The Random Access Memory (RAM) is selected by address lines A11--A15, refer to para 2.2.1. The CS input low selects the RAM. Signal NRDS low outputs the data from the location addressed by address lines A0—A10 onto data lines D0—D7. Signal NWDS low writes the data present on data lines D0—D7 into the location addressed by address lines A0—A10. When not selected the RAM data lines are high impedance.

2.9   DATA BUFFER

The Data Buffer Circuit controls the transfer of data between the CPU Data Bus and the Acorn Bus. The circuit consists of the bi-directional octal Bus Buffer IC12, exclusive OR gates IC16/6 and IC16/11, and NAND gate IC6/8, refer to Figure 12. The IC12 I/O lines are high impedance when the IC is not enabled.

For normal CPU operation the Bus Buffer is enabled for data transfers during the Phase 2 (§2) clock time, unless the ROM, RAM or VIA on the CPU Board is addressed, refer to Table 1 for truth table.

For DMA operation, the Bus Buffer is disabled for data transfers during the §2 clock time, when neither a ROM, nor a RAM address is present on the Acorn Bus address lines. The Bus Buffer is enabled by a ROM, or RAM address.

G	R/NW	OPERATION
Ø	Ø	B → A
Ø	1	B ← A
1	X	Isolation

X = Irrelevant
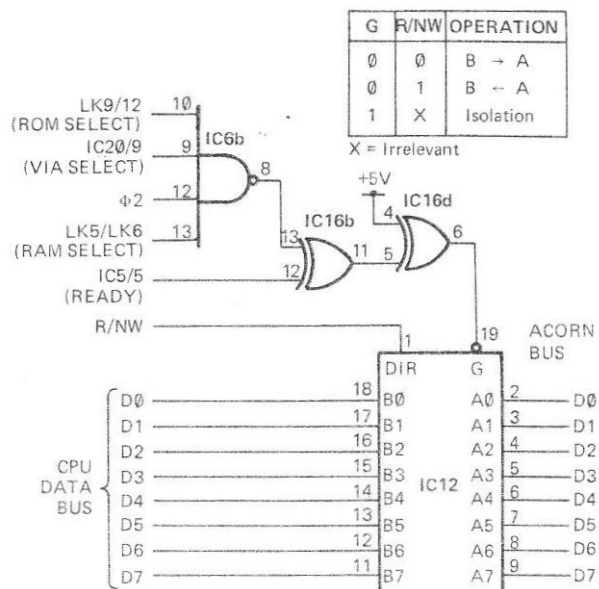
Figure 12. Data Buffer Circuit

READ Y	SELECT ROM	RAM	VIA	§2	IC16/13	12	11	IC12 G
1	1	1	1	1	0	1	1	0
1	X	X	X	0	1	1	0	1
1	0	X	X	X	1	1	0	1
1	X	0	X	X	1	1	2	1
1	X	X	0	X	1	1	0	1
0	1	1	1	1	0	0	0	1
0	X	X	X	0	1	0	1	0
0	0	X	X	X	1	0	1	0
0	X	0	X	X	1	0	1	0

X = Irrelevant

Table 1. Data Buffer Circuit Enable Conditions

When IC12 is enabled, the direction of data transfer is determined by the R/NW signal. R/NW high selects data transfer from the Acorn Bus (A input), to the CPU Data Bus (B output). R/NW low selects output from the CPU Data Bus (B input) to the Acorn Bus (A output). The Acorn Bus data lines D0—D7 are tied down to 0V by the Resistor Pack RP1.

2.10 VERSATILE INTERFACE ADAPTOR

The Versatile Interface Adaptor (VIA) is used to provide two Input/Output (I/O) Ports for the CPU Board. Port A (PA0—PA7) is connected to PL1 for use with a Keyboard, Port B (PB0—PB7) is connected to PL2 to provide a general purpose I/O Port on the Acorn Bus. Handshaking capability is provided by the control lines CA1, CA2, CB1 and CB2. Refer to block diagram, Figure 13.

The VIA is selected by address lines A9 and A10 both high at IC20b, when the Y1 output from IC20a is low, this selection allocates addresses 0E00 to 0FFF (hex) to the VIA. The functions of the VIA are then selected by address lines A0—A3, which are connected to the register select inputs RS0—RS3. The VIA has the following internal registers:

— Two Output Registers (OR), one for each Port.
— Two Input Registers (I R), one for each Port.
— Two Data Direction Registers (DDR), one for each Port.
— A Peripheral Control Register (PCR).
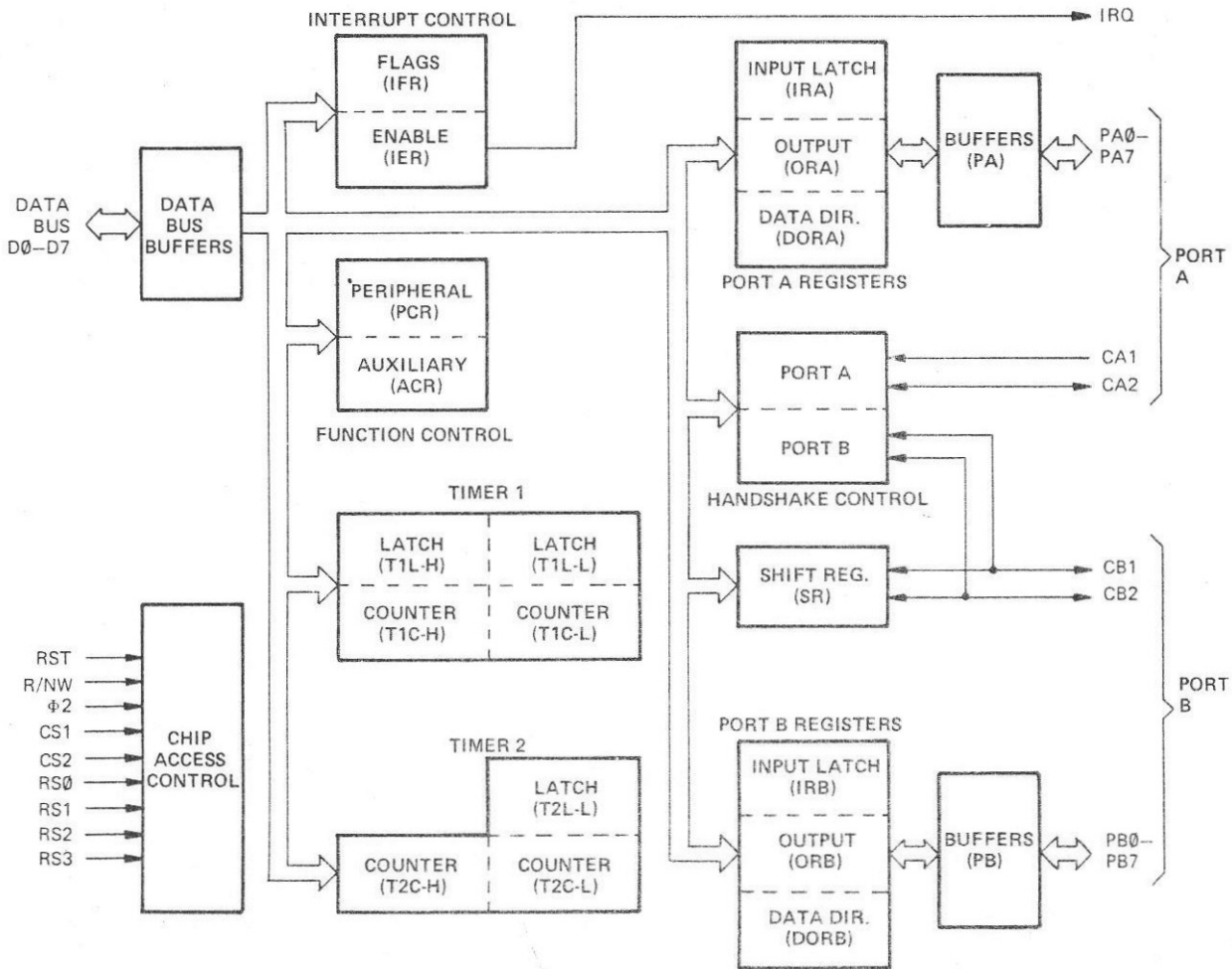
Figure 13. VIA Block Diagram
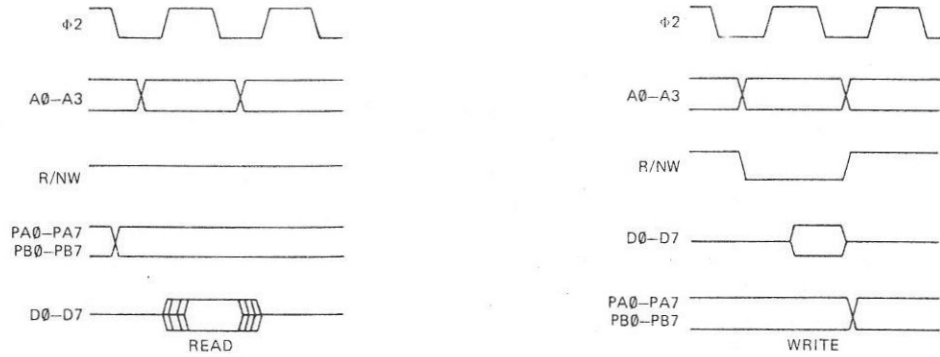
(a) CPU Timing
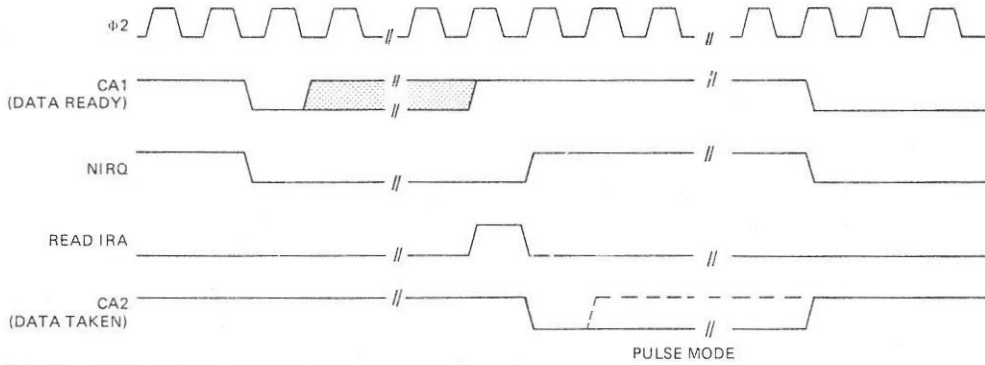
(b) Read Handshake Timing (Port A Only)
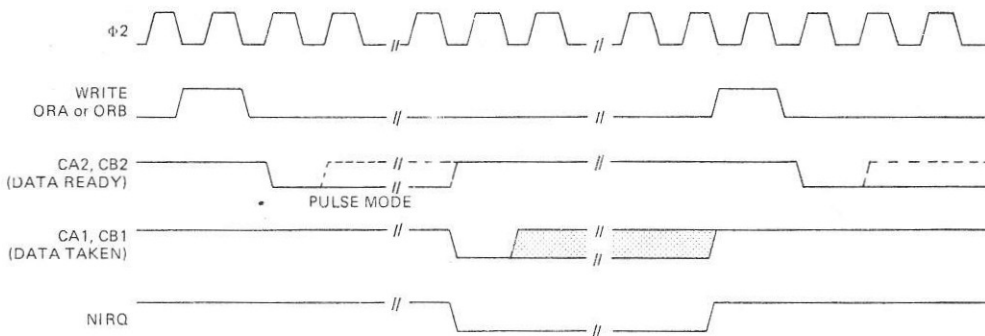
(c) Write Handshake Timing
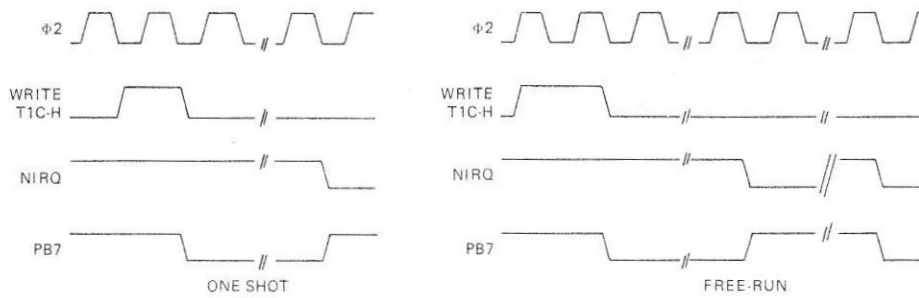
(d) T1 Operation

Figure 14. Typical VIA Operation Timing

An Auxiliary Control Register (ACR).
An Interrupt Flag Register (IFR).
An Interrupt Enable Register (IER).

The address selection of the registers is given in Table 2.

Hex	RS3	RS2	RS1	RSØ	Register	Remarks
Ø	Ø	Ø	Ø	Ø	ORB/IRB	Controls handshake Port B
1	Ø	Ø	Ø	1	ORA/IRA	Controls handshake Port A
2	Ø	Ø	1	Ø	DDRB	Program Port B I/O pins
3	Ø	Ø	1	1	DDRA	Program Port A I/O pins
4	Ø	1	Ø	Ø	T1L-L	Low order latch (Write)
					T1C-L	Low order counter (Read)
5	Ø	1	Ø	1	T1C-H	Refer to para 2.10.6
6	Ø	1	1	Ø	T1L-L	
7	Ø	1	1	1	T1L-H	
8	1	Ø	Ø	Ø	T2L-L	Low order latch (Write)
					T2C-L	Low order counter (Read)
9	1	Ø	Ø	1	T2C-H	Refer to para 2.10.7
A	1	Ø	1	Ø	SR	
B	1	Ø	1	1	ACR	
C	1	1	Ø	Ø	PCR	
D	1	1	Ø	1	IFR	
E	1	1	1	Ø	IER	
F	1	1	1	1	ORA	No effect on handshake

Table 2. VIA Register Selection

The VIA is also provided with two Timers T1 and T2, and an 8 bit Shift Register (SR). The Timers can be used to control the Port I/O lines to generate programmable-frequency square waves and/or to count externally generated pulses. The SR can be used to translate the 8 bit parallel data on D0—D7, to serial data on CB2 and vice versa,

The Reset (RST) input of the VIA is connected to the Power-on Reset Circuit. Signal NRST low clears all the internal registers to the '0' state, except T2 and SR. All I/O lines are set to input.

A timing diagram of some typical VIA operations is given on Figure 14. All timed operations are controlled by the 6502A CPU Board Phase 2 (§2) clock, except for serial data transfers when external clock mode is selected.

A link (LK10) is provided to connect the PA7 line from PL1 to the CA1 input, when Keyboard input operation under interrupt control is required.

2.10.1 Peripheral Control Register

The PCR is loaded by a microprocessor Write to the PCR address. The PCR is organized as shown on Figure 15. Table 3 gives the functions selected by PCR bits 1-3 for the Port A CA2 control line, the CA2 interrupt flag is IFR bit 0 (IFR0).

D	7	6	5	4	3	2	1	Ø
FUNCTION	CB2 Control			CB1 Control	CA2 Control			CA1 Control
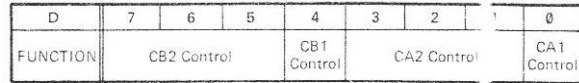
Figure 15. PCR Bit Significance

PCR BIT 3 2 1	FUNCTION
Ø Ø Ø	Input mode — Set CA2 interrupt flag (IFRØ) on a negative transition of the input signal. Clear IFRØ on a Read or Write of the Port A output Register.
Ø Ø 1	Independent Interrupt Input mode — Set IFRØ on a negative transition of the CA2 input signal. Reading or writing ORA does not clear the CA2 interrupt flag.
Ø 1 Ø	Input mode — Set CA2 interrupt flag on a positive transition of the CA2 input signal. Clear IFRØ with a Read or Write of the Port A Output Register.
Ø 1 1	Independent Interrupt Input mode — Set IFRØ on a positive transition of the CA2 input signal. Reading or writing ORA does not clear the CA2 Interrupt flag.
1 Ø Ø	Handshake Output mode — Set CA2 output low on a Read or Write of the Port A Output Register. Reset CA2 high with an active transition on CA1.
1 Ø 1	Pulse Output mode — CA2 goes low for one cycle following a Read or Write of the Port A Output Register.
1 1 Ø	Manual Output mode — The CA2 output is held low in this mode.
1 1 1	Manual Output mode — The CA2 output is held high in this mode.

Table 3 PCR Control Functions

3.8 EXEC COMMAND

Any file created in the same way as Boot (para 3.7.2) can be executed by the DOS command EXEC. If you still have your Boot file on disc set Option to Ø (see para 3.7.1) and enter EXEC BOOT (from DOS) or (from BASIC) enter *EXEC BOOT. The Boot file will now run with the same screen display as in para 3.7.2. The EXEC format is given in para 3.6.2.

3.9 QUALIFIERS

In para 2.5 the CAT command display showed that qualifier "space" was currently being used, and that all files had a space to the left of the colon (:) indicating that all files were allocated the qualifier "space".

The qualifier facility is a useful aid to file handling. It is implemented by means of the SET and USE DOS commands.

The SET command sets the current qualifier to any character until either the BREAK key is pressed, or the SET command is again used. Pressing the BREAK key sets the current qualifier to "space". Files are saved with the current qualifier (except when a file is saved immediately after a USE command). Note that no space is allowed between SET and the character, e.g. SETA is acceptable while SET A is not.

The USE command allows the next file operation to use other than the current qualifier. After the next file operation the qualifier reverts to the current qualifier.

The most common use of qualifiers is to separate files according to their content, e.g. qualifier B for BASIC programs and qualifier D for data files.

There may be two (or more) separate files with the same file name providing they are in separate qualifiers. Hence with the Assembler you can have a source file called, say, UADEØ1 in qualifier "space" which you will assemble into an object file with the same name providing it has a different qualifier.

3.10 SPOOLING

The SPOOL command will open a file for copying. To demonstrate you should enter:

    SPOOL SPFILE

or if you are in BASIC:

    *SPOOL SPFILE

For demonstration purposes, to put something in the file named SPFILE you could EXEC BOOT, see para 3.8 (or *EXEC BOOT if you are in BASIC).

To disable the SPOOL facility (closing the file) you must enter SHUT (or *SHUT SPFILE from BASIC).

You will need a small BASIC program to read your SPFILE, so re-enter BASIC and key in this program:

```
10 D=FIN "SPFILE"
20 C=EXTD
30a IF C=PTRD GOTO b
40 A=BGET D
50 IF A=10 PRINT $13
60 PRINT $A
70 GOTO a
80b SHUT D
90 END
```

Line 20 uses the EXT command to determine the length of the file. Line 30 checks to see if the end of file has been reached before reading in a character from the file. Line 50 tidies up the screen format, adding a Return to each Line Feed. Saving this file with the file name "SPREAD" will allow you to use it again. By changing the file name in Line 10 you can read any file.

3.11 DOS POINTER

When accessing files DOS maintains a pointer to the current access position within the file. The pointer can be read or changed by the BASIC PTR function. We used PTR in the SPREAD program (Line 30) in para 3.10 to exit from a loop when the end of file was reached. The pointer is set to "Ø" whenever a file is opened (FIN, FOUT' SPOOL, etc). We will look at the DOS Pointer again in para 6.1.

3.12 DISC TITLES

We can give the disc in the current drive a title using the command TITLE followed by a space and the disc name we are allocating (in BASIC the command is preceded by a *). Up to 13 characters may be used for a title.

3.13 INFORMATION ON FILES

3.13.1 INFO Command

We can read information on any file in the current drive using the INFO command (followed by a space and the file name). The information displayed is in the following form:

```
current    file  file  load     execution  length    start
qualifier  :lock name  address  address    in bytes  sector
```

```
    :  #BASIC  CØØØ  C2B2  Ø1ØØØ  ØØ2
    :  #LISP   28ØØ  28ØØ  Ø2ØØØ  Ø12
  s:  ZOMBY   3ØØØ  C2B2  ØØ312  Ø32
```

3.13.2 MON and NOMON Commands

The MON command turns on a message system which displays a file's information at each file access.

The NOMON command turns off the message system which was originally turned on by the MON command.

3.14 MACHINE CODE PROGRAM EXECUTION

To execute a machine code program the GO command may be used (followed by a space and the execution address). We used this command in para 2.9.5 to re-enter BASIC at C2B2 from DOS.

If the execution address is omitted the last known execution address will be used. Note that the current execution address is destroyed by CAT, and INFO does not set the execution address.

If a machine code program is on Drive Ø you can use the file name directly (as we called FORM4Ø and BASIC).

4. DOS COMMANDS AND ERROR MESSAGES

In the following commands, error and other messages, text, data and programs are said to be "displayed". They can, in fact be displayed on screen or printed or both, subject to the preceding Operating System control codes entered, see Table 1 in para 2.9.7.

File names and disc titles must be enclosed in quotes unless no spaces exist in file name. Only even numbers of quotes (or non at all) are allowed in file names or disc titles. Up to 13 characters are allowed in disc titles, and up to 7 characters are allowed in file names.

Legal drive numbers are dependent on the disc drive configuration, see para 2.6, but illegal drive numbers will simply cause the system to wait for the drive which is not there. Abbreviated command formats are shown following the full command formats.

4.1 DOS COMMANDS

`C A T` *(drive number)*

`. ` *(drive number)*

This command causes the Catalogue of drive *(drive number)*, (or the current drive if *(drive number)* is omitted) to appear on the screen.

A typical Catalogue will look like:

> ***CATØ**
> **Basic disc v1 drive Ø qual s opt Ø**
> : **#BASIC**   **#LISP**
> s: **ZOMBY**

The title of the disc is Basic disc v1; we are currently using drive Ø and qualifier s. The disc option is Ø (no auto-start features). Two files have been saved in qualifier "space", both of which have been locked to prevent careless deletion. One file has been saved in qualifier "s" and this has been left unlocked. The Catalogue is sorted alphabetically by qualifier and file name when it is output. The *(drive number)* can be omitted, or it must be Ø, 1, 2 or 3. If outside the range Ø to 3 then the message:

> **Drive ?**

will be displayed.

If the *(drive number)* is specified, the default drive for subsequent commands is changed to that specified.

`D E L E T E` *(file name)*

`D E .` *(file name)*

This command deletes the *(file name)* in the current qualifier from the current disc's Catalogue. If the entire disc is Write Protected a

> **Disc prot**

message is displayed. If the file is not found a

> **File ?**

message is displayed. If the file is Locked a

> **File prot**

message is displayed.

`D I R` *(drive number)*

`D .` *(drive number)*

This command causes the Catalogue of the drive *(drive number)* to be loaded into memory at hex start

When 0V is applied to PL1 pin 15, C2 is rapidly discharged via R3. The NRST signal is set low until the 0V is removed and C2 has charged again. Similarly, C2 discharges via D1 when the +5V supply is switched off or interrupted.

3.   SOFTWARE PARAMETERS

The following is a brief description of the software parameters affecting the CPU Board. Details are given of the 6502A Addressing Modes, Instruction Set and Interrupts, CPU memory addressing and the VIA software instructions.

3.1   6502A ADDRESSING MODES

The 6502A Microprocessor is provided with the following 13 Addressing Modes:

ACCUMULATOR ADDRESSING

This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING

In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

ABSOLUTE ADDRESSING

In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 64K bytes of addressable memory.

ZERO PAGE ADDRESSING

The Zero Page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the Zero Page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING — (X, Y INDEXING)

This form of addressing is used in conjunction with the Index Register and is referred to as "Zero Page, X" or " Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the Index Register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order of 8 bits of memory and crossing of page boundaries does not occur.

INDEX ABSOLUTE ADDRESSING --- (X, Y INDEXING)

This form of addressing is used in conjunction with X and Y Index Register and is referred to as "Absolute, X" and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the Index Register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

IMPLIED ADDRESSING

in the implied addressing mode, the address containing the operand is implicity stated in the operation code of the instruction.

RELATIVE ADDRESSING

Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the Program Counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING

In indexed indirect addressing (referred to as [Indirect, X]), the second byte of the instruction is added to the contents of the X index Register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the lower order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING

In indirect indexed addressing (referred to as [Indirect, Y]). the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y Index Register, the result being the low order eight bits of the effective address; The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT

The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the

MNEMONIC	OPERATION	IMMEDIATE OP	n	#	ABSOLUTE OP	n	#	ZERO PAGE OP	n	#	ACCUM OP	n	#	IMPLIED OP	n	#	(IND, X) OP	n	#	(IND), Y OP	n	#	Z PAGE, X OP	n	#	ABS, X OP	n	#	ABS, Y OP	n	#	RELATIVE OP	n	#	INDIRECT OP	n	#	Z PAGE, Y OP	n	#	PROCESSOR STATUS CODES 7 6 5 4 3 2 1 0 / N V . B D I Z C	MNEMONIC
A D C	A + M + C → A (4)(1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										N V . . . . Z C	A D C
A N D	A ∧ M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										N . . . . . Z .	A N D
A S L	C←[7 0]←0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													N . . . . . Z C	A S L
B C C	BRANCH ON C = 0 (2)																															90	2	2							. . . .	B C C
B C S	BRANCH ON C = 1 (2)																															B0	2	2							. . . .	B C S
B E Q	BRANCH ON Z = 1 (2)																															F0	2	2							. . . .	B E Q
B I T	A ∧ M				2C	4	3	24	3	2																															M₇ M₆ . . . . Z .	B I T
B M I	BRANCH ON N = 1 (2)																															30	2	2							. . . .	B M I
B N E	BRANCH ON Z = 0 (2)																															D0	2	2							. . . .	B N E
B P L	BRANCH ON N = 0 (2)																															10	2	2							. . . .	B P L
B R K	BREAK													00	7	1																									. . . . 1 . 1 .	B R K
B V C	BRANCH ON V = 0 (2)																															50	2	2							. . . .	B V C
B V S	BRANCH ON V = 1 (2)																															70	2	2							. . . .	B V S
C L C	0 → C													18	2	1																									 0	C L C
C L D	0 → D													D8	2	1																									. . . . 0 . . .	C L D
C L I	0 → I													58	2	1																									. . . . . 0 . .	C L I
C L V	0 → V													B8	2	1																									. 0	C L V
C M P	A − M	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										N . . . . . Z C	C M P
C P X	X − M	E0	2	2	EC	4	3	E4	3	2																															N . . . . . Z C	C P X
C P Y	Y − M	C0	2	2	CC	4	3	C4	3	2																															N . . . . . Z C	C P Y
D E C	M − 1 → M				CE	6	3	C6	5	2													D6	6	2	DE	7	3													N . . . . . Z .	D E C
D E X	X − 1 → X													CA	2	1																									N . . . . . Z .	D E X
D E Y	Y − 1 → Y													88	2	1																									N . . . . . Z .	D E Y
E O R	A ⊻ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										N . . . . . Z .	E O R
I N C	M + 1 → M				EE	6	3	E6	5	2													F6	6	2	FE	7	3													N . . . . . Z .	I N C
I N X	X + 1 → X													E8	2	1																									N . . . . . Z .	I N X
I N Y	Y + 1 → Y													C8	2	1																									N . . . . . Z .	I N Y
J M P	JUMP TO NEW LOC				4C	3	3																												6C	5	3				. . . .	J M P
J S R	JUMP SUB				20	6	3																																		. . . .	J S R
L D A	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										N . . . . . Z .	L D A
L D X	M → X (1)	A2	2	2	AE	4	3	A6	3	2																						BE	4	3							B6	4	2	N . . . . . Z .	L D X
L D Y	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3													N . . . . . Z .	L D Y
L S R	0→[7 0]→C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													0 . . . . . Z C	L S R
N O P	NO OPERATION													EA	2	1																									. . . .	N O P
O R A	A ∨ M → A (1)	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										N . . . . . Z .	O R A
P H A	A → Ms S − 1 → S													48	3	1																									. . . .	P H A
P H P	P → Ms S − 1 → S													08	3	1																									. . . .	P H P
P L A	S + 1 → S Ms → A													68	4	1																									N . . . . . Z .	P L A
P L P	S + 1 → S Ms → P													28	4	1																									(RESTORED)	P L P
R O L	←[7 0]←C←				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													N . . . . . Z C	R O L
R O R	→C→[7 0]→				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													N . . . . . Z C	R O R
R T I	RTRN INT													40	6	1																									(RESTORED)	R T I
R T S	RTRN SUB													60	6	1																									. . . .	R T S
S B C	A − M − C → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3										N V . . . . Z (3)	S B C
S E C	1 → C													38	2	1																									 1	S E C
S E D	1 → D													F8	2	1																									. . . . 1 . . .	S E D
S E I	1 → I													78	2	1																									. . . . . 1 . .	S E I
S T A	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3										. . . .	S T A
S T X	X → M				8E	4	3	86	3	2																												96	4	2	. . . .	S T X
S T Y	Y → M				8C	4	3	84	3	2													94	4	2																. . . .	S T Y
T A X	A → X													AA	2	1																									N . . . . . Z .	T A X
T A Y	A → Y													A8	2	1																									N . . . . . Z .	T A Y
T S X	S → X													BA	2	1																									N . . . . . Z .	T S X
T X A	X → A													8A	2	1																									N . . . . . Z .	T X A
T X S	X → S													9A	2	1																									. . . .	T X S
T Y A	Y → A													98	2	1																									N . . . . . Z .	T Y A

(1) ADD 1 to `N` IF PAGE BOUNDARY IS CROSSED
(2) ADD 1 TO `N` IF BRANCH OCCURS TO SAME PAGE
     ADD 2 TO `N` IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT = BORROW
(4) IF IN DECIMAL MODE Z FLAG IS INVALID
     ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X	INDEX X	+	ADD	M₇	MEMORY BIT 7
Y	INDEX Y	−	SUBTRACT	M₆	MEMORY BIT 6
A	ACCUMULATOR	∧	AND	n	NO. CYCLES
M	MEMORY PER EFFECTIVE ADDRESS	∨	OR	#	NO. BYTES
Ms	MEMORY PER STACK POINTER	⊻	EXCLUSIVE OR		

Table 6.   Instruction Set Coding

third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the Program Counter.

3.2   6502A INSTRUCTION SET

The following Instruction Set is used by the 6502.A:

ADC   Add Memory to Accumulator with Carry
AND   "AND" Memory with Accumulator
ASL   Shift left One Bit (Memory or Accumulator)
BCC   Branch on Carry Clear
BCS   Branch on Carry Set
BEQ   Branch on Result Zero
BIT   Test Bits in Memory with Accumulator
BMI   Branch on Result Minus
BNE   Branch on Result Not Zero
BPL   Branch on Result Plus
BRK   Force Break
BVC   Branch on Overflow Clear
BVS   Branch on Overflow Set
CLC   Clear Carry Flag
CLD   Clear Decimal Mode
CLI   Clear Interrupt Disable Bit
CLV   Clear Overflow Flag
CMP   Compare Memory and Accumulator
CPX   Compare Memory and Index X
CPY   Compare Memory and Index Y
DEC   Decrement Memory by One
DEX   Decrement Index X by One
DEY   Decrement Index Y by One
EOR   "Exclusive or" Memory with Accumulator
INC   Increment Memory by One
INX   Increment Memory X by One
INY   Increment Memory Y by One
JMP   Jump to New Location
JSR   Jump to New Location Saving Return Address
LDA   Load Accumulator with Memory
LDX   Load Index X with Memory
LDY   Load Index Y with Memory
LSR   Shift One Bit Right (Memory or Accumulator)
NOP   No Operation
ORA   "OR" Memory with Accumulator
PHA   Push Accumulator on Stack
PHP   Push Processor Status on Stack
PLA   Pull Accumulator from Stack
PLP   Pull Processor Status from Stack
ROL   Rotate One Bit Left (Memory or Accumulator)
ROR   Rotate One Bit Right (Memory or Accumulator)

RTI   Return from Interrupt
RTS   Return from Subroutine
SBC   Subtract Memory from Accumulator with Borrow
SEC   Set Carry Flag
SED   Set Decimal Mode
SEI   Set Interrupt Disable Status
STA   Store Accumulator in Memory
STX   Store Index X in Memory
STY   Store index Y in Memory

TAX   Transfer Accumulator to Index X
TAY   Transfer Accumulator to Index Y
TSX   Transfer Stack Pointer to Index X
TXA   Transfer Index X to Accumulator
TXS   Transfer Index X to Stack Register
TYA   Transfer Index Y to Accumulator

The coding, number of cycle and number of bytes for each address mode, together with the status codes are given on Table 6.

3.3   6502A INTERRUPTS AND RESET

The 6502A microprocessor has two interrupt signal inputs NIRQ and NNMI and a reset input NRST. These inputs are used to load vectored addresses into the PC. The instructions located at the addresses are the first instructions of the relevant interrupt or start routine.

3.3.1   Interrupt Request

A low level on the NIRQ input will initiate an interrupt sequence at the end of the current instruction, provided that the interrupt mask bit (I) in the Processor Status Register (P) is '0'. The contents of the Program Counter (PC) and the P Register are stored in the stack. The I bit is then set to '1' in the P Register. At the end of this cycle the PCL byte is loaded from address FFFE (hex) and the PCH byte is loaded from address FFFF (hex), transferring program control to the memory vector located at these addresses.

3.3.2   Non-Maskable Interrupt

A negative going edge on the NNMI input will initiate an interrupt sequence at the end of the current instruction, the P Register I bit has no effect. The sequence is as described for NIRQ, except that PC is loaded from addresses FFFA (hex) and FFFB (hex).

3.3.3   Reset

The NRST input low inihibits microprocessor operation. When a positive edge is detected the microprocessor starts the reset sequence. After the system initialization time of six clock cycles, the P Register I bit is set to a '1'. The PC is loaded from addresses

FFFC (hex) and FFFD (hex), transferring program control to the memory vector located at these addresses.

3.4 CPU MEMORY ADDRESSING

The CPU RAM and ROM are assigned to the addresses shown in the Acorn Memory Map, Figure 20. The different types of ROM are selected by means of the links fitted to the DIL header that is inserted in LK9, refer to pare 2.2.2. The 1K or 2K RAM option 1 is selected by LK5 and LK6, refer to Para 2.2. IC13 may also be used for a ROM IC instead of a RAM IC.
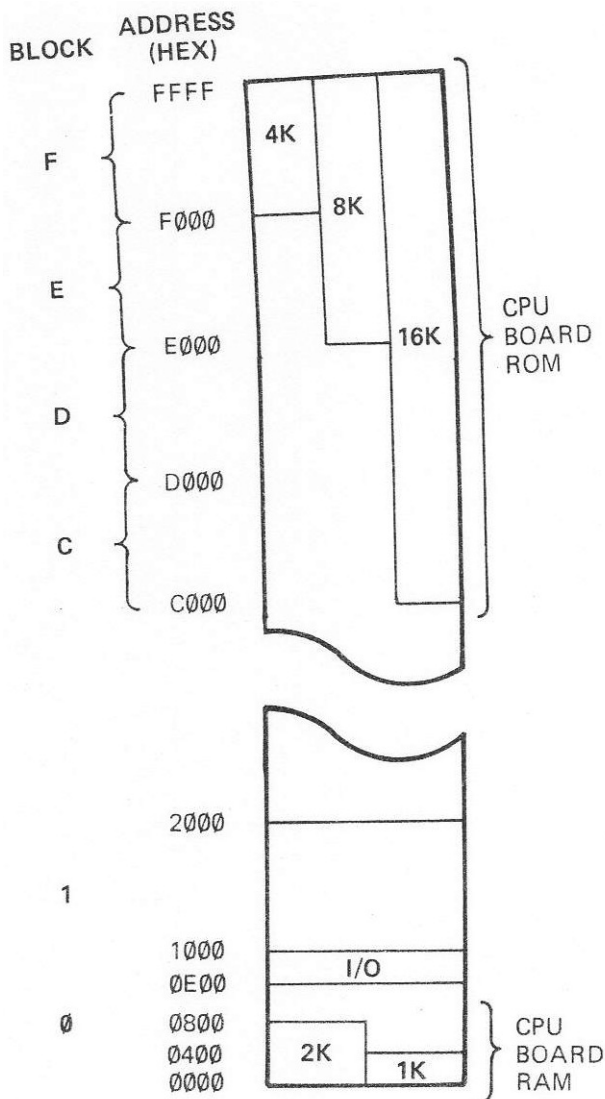

Figure 20. 5502A CPU Memory Map

3.5 VIA SOFTWARE INSTRUCTIONS

The operation of the VIA is controlled by program instructions from the microprocessor. The VIA is

assigned addresses 0E20 to 0E2F (hex) , although because of incomplete decoding on the CPU Board, the address block 0E00 to 0FFF (hex) can only be used for the VIA, The VIA Register addressing is given on Table 7. The two Ports of the VIA are designated Port A and Port B.

ADDRESS BITS				R/NW	REGISTER	FUNCTION
A3	A2	A1	A0			
0	0	0	0	1	IRB	Input Register B
0	0	0	0	0	ORB	Output Register B
0	0	0	1	1	IRA	Input Register A
0	0	0	1	0	ORA	Output Register A
0	0	1	0	—	DDRB	Data Direction Register B
0	0	1	1	—	DDRA	Data Direction Register A
0	1	0	0	1	T1C-L	T1 Low Order Counter
0	1	0	0	0	T1L-L	T1 Low Order Latch
0	1	0	1	—	T1C-H	T1 High Order Counter
0	1	1	0	—	T1L-L	T1 Low Order Latch
0	1	1	1	—	T1L-H	T1 High Order Latch
1	0	0	0	1	T2C-L	T2 Low Order Counter
1	0	0	0	0	T2L-L	T2 Low Order Latch
1	0	0	1	—	T2C-H	T2 High Order Counter
1	0	1	0	—	SR	Shift Register
1	0	1	1	—	ACR	Auxiliary Control Register
1	1	0	0	—	PCR	Peripheral Control Register
1	1	0	1	—	IFR	Interrupt Flag Register
1	1	1	0	—	IER	Interrupt Enable Register
1	1	1	1	1	IRA	Input Register A (no handshaking)
1	1	1	1	0	ORA	Output Register A (no handshaking)

Table 7. VIA Address Allocation

3.5.1 Data Input/Output

The selection of the input/output pins of both Ports is controlled by the Data Direction Registers (DDRA, DDRB). A pin is selected for input or output by the corresponding bit in the DDR, input is selected by a '0' hit, output by a '1' bit.

The data bits to be output from a Port are loaded into the corresponding Output Register (ORA, ORB). The bits are set onto the Port output lines at the end of the Write instruction. Writing to a pin selected for input loads the Output Register bit, but. has no effect on the output pin.

The Input Registers (IRA, IRB) are loaded by the corresponding CA1 or CB1 signal, when input latching is enabled by the control bit in the ACR. A microprocessor Read operation then reads the contents of the IR. When input latching is disabled, a Read operation reads the current state of the Port input pin.

"Handshaking" is available on Port A for both input and output, but only for output on Port B. Handshaking signals are controlled automatically by Reading or Writing to Port A or Port B Registers, RS0—RS3 = 0 or 1 (hex). When Writing or Reading to Port A Registers with RS0—RS3 = F (hex), handshaking is disabled.

The handshaking signal operation is defined by the appropriate bits of the PCR, refer to para 2.10.1.

3.5.2   Timer 1

Timer 1 is controlled by the ACR, refer to para 2.10.2. For a single timed interrupt operation, Timer 1 is set by loading the Low Order Latch T1L-L and then the High Order Counter T1C-H. The contents of T1L-L are loaded into Counter T1C-L by the action of loading T1C-H. T1 is counted down to zero by the $\S2$ clock. When zero is reached the interrupt flag IFR6 is set and, if interrupt enable IER6 is a '1', signal NIRQ is set low. IFR6 is reset by writing to T1C-H, or reading T1C-L.

For continuous interrupt (free-run) operation the Latch T1L-H has to be loaded as well as the Counter T1C-H. When T1 counts down to zero in this mode, T1C-L and T1C-H are reloaded from T1L-L and T1L-H, to restart the count down cycle.

When the PB7 output pin is selected for a single pulse operation, T1 operates as described above. A negative pulse is generated on PB7 for the duration of the timed interrupt. The pulse length = $(n + 1.5) \S2$, where n is the number loaded in the Counter. The DDRB bit 7 must be 1 for PB7 to function as an output.

For a square wave output on PB7, T1 operates in the free-run mode as described above. PB7 is low for $(n + 1.5) \S2$ and high for $(n + 2) \S2$.

The T1 Latches may be loaded with a different number, while the Counters are counting down. When in the free-run mode, the new value is loaded into the Counters, when the count down reaches zero. If PB7 output is selected the output can thus be a complex waveform.

3.5.3   Timer 2

Timer 2 is controlled by the ACR, refer to para 2.10.2.

The T2 single timed interrupt operation is similar to that described for T1. The T2 interrupt flag is IFR5 and the interrupt enable IER5, After the count down the Counters roll over to all '1's and continue counting. The Counters can be read to determine how long the interrupt has been set. Reading T2C-L resets the interrupt flag IFR5. Writing to T2C-H also clears IFR5. T2 does not have a High Order Latch.

The T2 Low Order Latch T2L-L is also used to control Shift Register operations in the following modes:

-     Shift in under T2 control.
-     Free-running output at rate determined by T2.
-     Shift out under T2 control.

For further details, refer to Shift Register Operation para 3.5.4.

In the pulse counting mode T2 is counted down from a number (loaded into the Counters as described above) by negative going pulses on input PB6. The DDRB bit 6 must be set to '0' to select input. When T2 = '0' IFR5 is set and, if IER5 is a '1', signal NIRQ is set low. Writing to T2C-H clears IFR5.

3.5.4   Shift Register Operation

The SR has eight operating modes that are controlled by setting the ACR bits 2, 3 and 4, refer to para. 2.10.3. The SR interrupt flag IFR bit 2 (IFR2) is used to request a data byte from the microprocessor, or signal that a data byte can be read from the SR. When the interrupt enable IER2 is '1', setting IFR2 sets signal NIRQ low. IFR2 is cleared by Writing to or Reading the SR. When the SR is disabled, ACR bits 2-4 = '000', CB1 and CB2 are controlled by the PCR and IFR2 is held at '0'.

For serial data input or output on C82, the data bits are clocked in or out under the control of either an internal clock or an external clock input on CB1 as follows:

- *Input, T2 clock control.* The clock output on CB1 is a square wave of period $2 (n + 2) \S2$, where n is the number-stored in T2L-L. Transfer is initiated by a Write or Read to the SR. The data bit on CB2 is shifted into the SR by the $\S2$ clock cycle following the positive going edge on CB1. After 8 CB1 pulses IFR2 is set.

- *Input, $\S2$ clock control,* The clock output on CB1 is $\S2$ divided by 2. Transfer is initiated

by a Read or Write to the SR. The clock on CB1 stops after 8 pulses and IFR2 is set.

- *Input, external clock control.* The SR is loaded with the data bit on CB2 by the first §2 clock cycle after the positive going clock edge on CB1. The SR sets IFR2 after 8 clock pulses.

- *Output, T2 control free-running.* The 8 bits stored in the SR are clocked onto CB2 repetitively. The clock period on CB1 is 2 (n + 2) §2, where n is the number stored in T2L-L. Signal NIRQ is not set. Transmission is initiated by a Write to the SR.

- *Output, T2 clock control.* The 8 bits loaded in the SR are clocked onto CB2. The clock period on CB1 is 2(n + 2) §2, where n is the number stored in T2L-L. Transmission is initiated by a Write to the SR. When the 8 data bits have been sent IFR2 is set.

- *Output, §2 clock control.* The clock output on CB1 is §2 divided by 2. The 8 bits loaded in the SR are clocked onto CB2. Transmission is initiated by a Write to the SR. When the 8 data bits have been sent IFR2 is set.

- *Output, external clock control.* The 8 bits loaded in SR are clocked onto CB2 by the first §2 clock cycle after the negative going edge of the external clock input on. CB1. Transmission is initiated by Writing to the SR. When 8 clock pulses have been counted IFR2 is set.

3.5.5 Interrupt Operation

The IFR flags are set by the various functions in the VIA. When a flag is set IFR bit 7 is set to indicate an interrupt condition. Setting a flag sets the NIRQ output low, provided that the corresponding IER bit is set. The IFR can be read by the microprocessor. An IFR flag can be reset by Writing a '1' to the appropriate IFR bit.

The IER flags are set to enable the corresponding IFR flags by Writing to the IER with a '1' in bit 7 and '1's corresponding to the flags. An IER flag can be reset by Writing to the IER with a '0' in bit 7 and a '1' corresponding to the flag. The setting of the IER flags can be read by the microprocessor, bit 7 will be read as a 'I',

4.   6502A CPU CONNECTIONS

4.1   6502A CPU BOARD TO ACORN BUS (PL2)

Pin Side A	Mnemonic	Meaning	I/O
1	+5V	+5V Board Supply	I
2	A15		
3	A14	Addr ss Lines	I/O
4	NWDS	Write Data Strobe	I/O
5	NRDS	Read Data Strobe	I/O
6	NRST	Reset	O
7	A8		
8	A7		
9	A6		
1Ø	A5		
11	A4	Address Lines	I/O
12	A3		
13	A2		
14	A1		
15	AØ		
16	D7		
17	D6		
18	D5		
19	D4		
2Ø	D3	Data Lines	I/O
21	D2		
22	D1		
23	DØ		
24	A13		
25	A12		
26	A11	Address Lines	I/O
27	A1Ø		
28	A9		
29	Φ2	Phase 2 Clock	O
3Ø	R/NW	Read/Write Control Line	I/O
31	NBLKØ	Block Ø Address Select	O
32	0V	0V Board Supply	I

Pin Side B	Mnemonic	Meaning	I/O
1			
2			
3	PB7		
4	PB6		
5	PB5		
6	PB4		
7	PB3	Port B Data Lines	I/O
8	PB2		
9	PB1		
1Ø	PBØ		
11	CB2		
12	CB1	Port B Control Lines	I/O

Pin Side B	Mnemonic	Meaning	I/O
13	12MHz		
14	8MHz		
15	6MHz		
16	4MHz	Clock Signals	O
17	3MHz		
18	2MHz		
19			
20			
21	1MHz	Clock Signal	O
22	NBGt	Bus Grant	O
23			
24			
25	NBRq	Bus Request	I
26	MR	Memory Ready	I
27			
28	NIRQ	Interrupt Request	I
29	NNMI	Non-Maskable Interrupt	I
30	SYNC	Microprocessor Instruction Fetch	O
31			
32	0V	0V Board Supply	I

4.2 6502A CPU BOARD TO I/O UNIT (PL1)

Pin	Mnemonic	Meaning	I/O
1	CA1	Port A Control Lines	I/O
2	CA2		
3			
4			
5			
6			
7			
8	Φ2	Phase 2 Clock	O
9			
10	PA0	Port A Data Line	I/O
11	0V	0V Supply	O
12	PA1	Port A Data Line	I/O
13	+5V	+5V Supply	O
14	PA2	Port A Data Line	I/O
15	RESET	System Reset	I
16	PA3		
17	PA7		
18	PA4	Port A Data Lines	I/O
19	PA6		
20	PA5		

5. PARTS LIST

5.1 MECHANICAL PARTS

ITEM	DESCRIPTION	VALUE	QTY	PART NO.
	Printed Circuit Board 200,005		1	
	14 Pin IC Socket		9	
	16 Pin IC Socket		5	
	20 Pin IC Socket		3	
	24 Pin IC Socket		1	
	28 Pin IC Socket		1	
	40 Pin IC Socket		2	
	16 Pin DIL Header		1	
	2 Pin Links	Molex 22-03-2021	6	
	Molex Mini-Shunts	7859-2	6	

5.2 ELECTRICAL PARTS

ITEM	DESCRIPTION	VALUE	QTY	PART NO.
C1	Capacitor Electrolytic	22μF 16V	1	
C2	Capacitor Electrolytic, Tantalum Bead	10μF 16V	1	
C3	Capacitor Ceramic Disc	100pF	1	
C4...C9	Capacitor Ceramic	47nF	6	

ITEM	DESCRIPTION	VALUE	QTY	PART NO.
PL1	Connector 20 Way, Right Angle Plug Solder Tail	3M 3428-1302		
PL2	Connector 64 Way, Right Angle Plug Solder Tail	DIN 41612		
D1	Diode	IN4148	1	
IC1	Integrated Circuit	74S04	1	
IC2...IC4	Integrated Circuit	74S163	3	
IC5	Integrated Circuit	74LS74	1	
IC6	Integrated Circuit	74LS20	1	
IC7	Integrated Circuit	SY6522A	1	
IC8	Integrated Circuit	SY6502A	1	
IC9, IC10	Integrated Circuit	74 LS244	2	
IC11	Integrated Circuit	*	1	
IC12	integrated Circuit	74LS245	1	
IC13	Integrated Circuit	6116LP-4	1	
IC14	Integrated Circuit	74LS04	1	
IC15	Integrated Circuit	74LS125	1	
IC16	Integrated Circuit	74LS86	1	
IC17	Integrated Circuit	74LS32	1	
IC18	Integrated Circuit	74LS132	1	
IC19	Integrated Circuit	74LS20	1	
IC20	Integrated Circuit	74LS139	1	

* PROM supplied in accordance with System requirements.

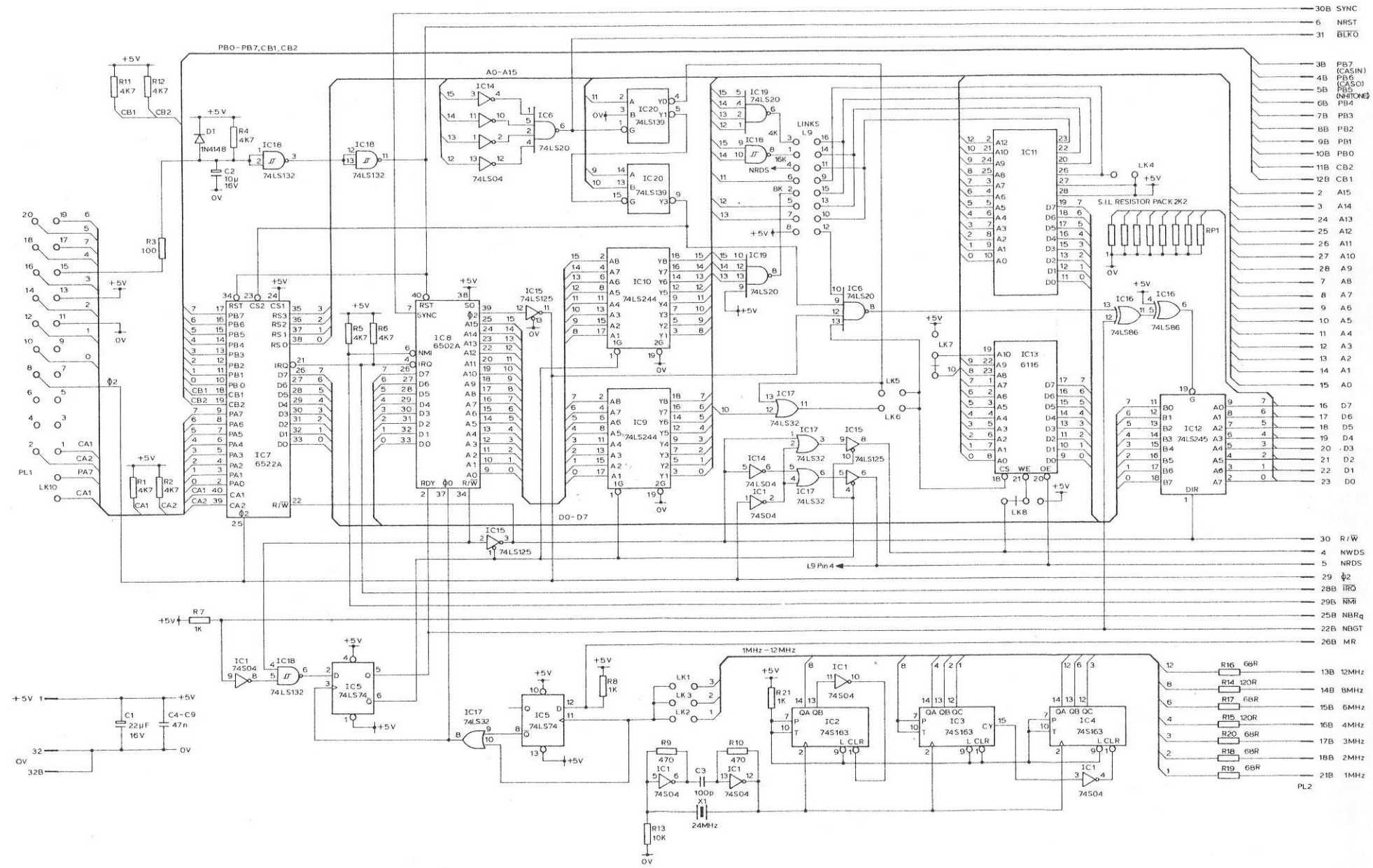| ITEM	DESCRIPTION	VALUE	QTY	PART NO.
R1, R2	Resistor	4,7kOhm	2	
R3	Resistor	100Ohm	1	
R4...R6	Resistor	4.7kOhm	3	
R7, R8	Resistor	1kOhm	2	
R9, R10	Resistor	470Ohm	2	
R11, R12	Resistor	4.7kOhm	2	
R13	Resistor	10kOhm	1	
R14...R20	Resistor	68Ohm	7	
R21	Resistor	1kOhm	1	
RP1	Resistor Pack SI L 850-91-2K2 AB		1	
X1	Crystal 24MHz (Fun. amental)		1	

Figure 21 6502A CPU Board Circuit Diagram